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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,195	09/10/2003	Kenichiro Uda	56937-089	3242

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,195	UDA, KENICHIRO	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 7-12 and 14* is/are rejected.

7)☒ Claim(s) *5,6 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/658,195 filed 09/10/2003 and amendment filed 06/29/2006.

2. Claims 1-12, 14 and 15 are pending in the Application.

3. Applicant's arguments have been fully considered and are persuasive. However, upon further consideration, a new ground(s) of rejection is made in view of Hirabayashi et al. (US Patent 5,345,098).

Claim Objections

4. Claim 1, 14 are objected to because of the following informalities:

claim 1 on line 9 has either redundancy or unfinished phrase, such as "and the power supply side of a potential"

claim 14 contains the limitation which is redundant to the last limitation of the claim 1, from which depends.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 7-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosegawa et al. (US Patent 6,028,580) in view of Hirabayashi et al. (US Patent 5,345,098).

With respect to claim 1 Kosegawa et al. teaches a structure of a power supply path utilized in the design of an integrated circuit (within integrated circuit design (abstract)), wherein in every cell in the integrated circuit, a power supply path on a power supply side of a high potential and a power supply path on a power supply side of a low potential are provided opposite each other and wherein in every cell in the integrated circuit, the power supply path on the power supply side of the high potential and the power supply path on the power supply side of the low potential (as shown on the Fig. 1(a) a high potential power source V_{dd} 15 and a low potential power source V_{ss} 16 disposed on a opposite sides from each other (col. 8, ll.29-30)), each comprise: a main power line (within main line 15a disposed on the power source line 15 on the side of the high potential power source V_{dd} (col. 8, ll.58-612) and main line 16a disposed on the power source 16 on the low potential power source V_{ss} (col. 9, ll.3-4)); a plurality of outgoing power lines branching off from the main power line (within plurality of branched wiring sections 15b (outgoing power lines) as shown on the Fig. 1(a) outgoing from main power line 15 (col. 8, l.67; col. 9, ll.1-2)), wherein a plurality of pitches between adjacent outgoing power lines of the plurality of branched outgoing lines in the longitudinal direction of the main line are set so as to be equal to each other (as might be seen on the Fig. 1(a) the distance (pitch) between main power source line 15 on the side of the high potential power source V_{dd} and main power source line 16 on the side of the low potential power source V_{ss} composed symmetrically, wherein plurality of pitches (distances between branches 15b and branches 16b) are set equal to each other). However Kosegawa et al. lacks the specifics regarding pitches as claimed. Hirabayashi

et al. teaches a power supply structure of the gate arrays, wherein the power branch off from the main power line region formed on the external cell array region and pass into the internal cell array region are formed to be located at **predetermined intervals with respect to the regularly arranged internal cells** (col. 1, ll.25-39; col. 2, ll.1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Hirabayashi et al. to teach the specifics subject matter Kosegawa et al. does not teach, because the power lines which branch off from the main power line formed to be located **at predetermined intervals** with respect to the regularly arranged internal cells (col. 1, ll.25-30).

With respect to claims 2-4, 7-12 and 14 Kosegawa et al. teaches:

Claim 2: wherein branching positions of the plurality of outgoing power lines of the power supply path on the power supply side of the high potential correspond to branching positions of the plurality of outgoing power lines of the power supply path on the power supply side of the low potential in the longitudinal direction of the power supply paths as shown on the Fig. 1(a), wherein branching positions of the outgoing power lines 15 b of the power supply path 15a on the high potential 15 correspond to the branching positions of the outgoing power lines 16 b of the power supply path 16a on the high potential 16;

Claims 3 and 4: wherein lengths of the respective plurality of outgoing power lines are set so as to be equal to each other in both the power supply paths on the power supply sides of the high potential and the low potential, respectively as shown on the Fig. 1(a), wherein outgoing power lines 15b on the power supply sides of the high

potential and outgoing power lines 16b on the power supply sides of the low potential are equal;

Claims 7-12: wherein widths of the respective plurality of outgoing power lines are equal to each other and set so as to be smaller than distances between the adjacent outgoing power lines of both the power supply paths on the power supply sides of the high potential and the low potential, respectively as might be seen on the Fig. 1(a) the length and width of the outgoing power lines 15b and 16b are smaller than distances between them on both sides of the power main lines 15a and 16a, which are high potential and low potential respectively, wherein their width has arranged with certain relationship with the size of the element, to which power is supplied with the consideration of the design rules (col. 9, ll.37-40);

Claim 14: wherein the pitches between adjacent outgoing power lines of the power supply path on the power supply side of the high potential and the pitches between adjacent outgoing power lines of the power supply path on the power supply side of the low potential are set so as to be equal to each other (as shown on the Fig. 1(a) the distance (pitch) between main power source line 15 on the side of the high potential power source V_{dd} and main power source line 16 on the side of the low potential power source V_{ss} composed symmetrically, wherein plurality of pitches (distances between branches 15b and branches 16b) are set equal to each other).

However Kosegawa et al. lacks the specifics regarding pitches as claimed. Hirabayashi et al. teaches a power supply structure of the gate arrays, wherein the power branch off from the main power line region formed on the external cell array

region and pass into the internal cell array region are formed to be located at **predetermined intervals with respect to the regularly arranged internal cells** (col. 1, ll.25-39; col. 2, ll.1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Hirabayashi et al. to teach the specifics subject matter Kosegawa et al. does not teach, because the power lines which branch off from the main power line formed to be located **at predetermined intervals** with respect to the regularly arranged internal cells (col. 1, ll.25-30).

Allowable Subject Matter

7. Claims 5, 6 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach a structure of a power supply path in the design of an integrated circuit, wherein lengths of the plurality of outgoing power lines of the power supply path on the high potential are set as to be longer than length of the plurality of outgoing power lines of the power supply path on the low potential; the pitch between the main power line of the power supply path on the power supply side of the high potential and the main power line of the power supply path on the power supply side of the low potential is set to be longer than sum of the length of an outgoing line of the power supply side of the high potential and the length of an outgoing line of the power supply side of the low potential provided opposite the outgoing line of the power supply side of the high potential.

Remarks

8. In response to the Applicant's argument "Kosegawa fails to disclose a structure of a power supply path utilized in the design of an integrated circuit wherein in every cell in the IC a plurality of pitches between adjacent outgoing power lines of the plurality of branched outgoing lines in the longitudinal direction of the main line are set so as to be equal to each other", Examiner respectfully disagrees for the following reasons. Kosegawa discloses a power source line and an output line connected to the **plurality** of thin film **transistors,** and main wiring section and a branched wiring section branched into respective transistors (abstract). Additionally, Hirabayashi et al. teaches a power supply structure of the gate arrays, wherein the power branch off from the main power line region formed on the external cell array region and pass into the internal cell array region are formed to be located at **predetermined intervals with respect to the regularly arranged internal cells** (col. 1, ll.25-39; col. 2, ll.1-5).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner
Helen Rossoshek
Art Unit 2825

A. M. Thompson
Primary Examiner
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